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ANALYSIS OF EFFICIENT CARRY SELECT ADDER USING BRENT KUNG ADDER

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ABSTRACT

Adders are the basic building blocks in a digital circuit design. It is used to perform the additions of two n-bit numbers. Adders find its applications in areas like microprocessor, digital signal processing and even in data path logic operations. Performance of a circuit is mainly determined by the speed of addition. To perform fast arithmetic operations, high speed adders combined with parallel prefix adder architectures are used. Instead of using Ripple Carry Adder (RCA), here a parallel prefix adder i.e. Brent Kung (BK) adder is used with carry select adder for obtaining better performance. The Brent Kung adder offers the best performance when compared with the other parallel prefix adders and it reduces the delay of a conventional RCA. Four architecture structures namely Regular Linear BK CSA, Regular Modified BK CSA, Regular SQRT BK CSA and Modified SQRT BK CSA are designed so as to analyze and to compare the performance in terms of area, power and delay. From the analysis, it is clear that modified SQRT Brent Kung Carry Select Adder gives better results than other adder architectures. The designs have been simulated using Tanner EDA tool.

Keywords: *Ripple Carry Adder, BK CSA, SQRT Brent Kung, Tanner EDA tool.*

INTRODUCTION

Adders in Digital Design: Addition is one of the four elementary operations in mathematics, the other being subtraction, multiplication and division. In digital systems, addition forms the most important operation. This is primarily because we can perform operations like subtraction, multiplication and division using the addition operation. Hence the design of a very fast, accurate and a lower power consumption adder directly results in the increased speed of the device for faster computational purpose as well as an improved life. Design of high speed digital adders with efficient area and power is one of the important areas of research in VLSI system design. In digital adder circuits, the speed of addition is limited by the time required for a carry to propagate through the adder. (Vasanthy and Jeganathan 2007, Vasanthy et.al., 2008, Raajasubramanian et.al., 2011, Jeganathan et.al., 2012, 2014, , Sridhar et.al., 2012, Gunaselvi

et.al., 2014 & 2020, Premalatha et.al., 2015, Seshadri et.al., 2015, Shakila et.al., 2015, Ashok et.al., 2016, Satheesh Kumar et.al., 2016).

Brent-Kung Adder: The Brent-Kung (BK) adder in 1982 was proposed to resolve the drawbacks in Kogge Stone (KS) adder. It is one of the parallel prefix adders. Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. Brent-Kung approach focused on optimal area design issue to have the minimal number of nodes at the cost of maximum logic depth. The block diagram of 4-bit Brent-Kung adder is shown in Fig 1

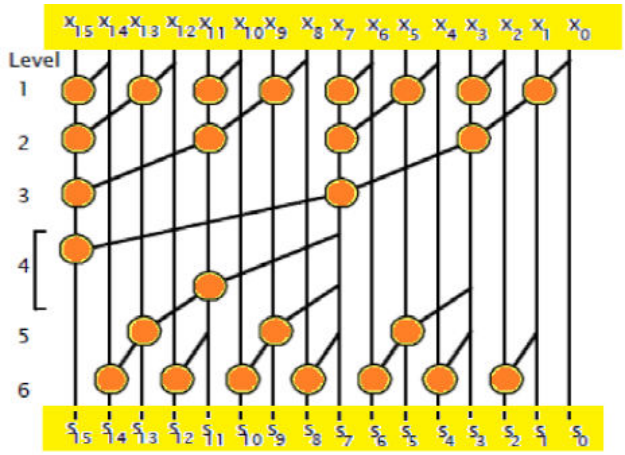

Fig 1: Brent Kung Adder

Kogge-Stone adder: The schematic of Kogge Stone Adder is shown in Fig 2. It is widely used in high performance applications. The general concept of Kogge Stone adder is almost the same as that of the carry look ahead adder except for the second step, called parallel carry prefix chain. In the first level (L=1), generates and propagates of 2-bit are computed at the same time. In the second level (k=2), generates and propagates of 4-bit are calculated by using the result of 2-bit in level 1. Therefore, the actual carry-out value of the 4th bit would be available while the calculations in level 2 are being computed. In the third level (L=3), the carry-out of the 8th bit is computed by using the 4th bit carry result. In Figure 1.8, red boxes are propagate (P) and generate (G) generators for each bit of two inputs. Yellow boxes contain propagate block and generate block and the delay of one yellow box is equal to two gate delay (D). The blue boxes keep the original generate value transmitted from the previous level. In each level, because all carries are calculated in parallel, the delay is the running time of single yellow box.

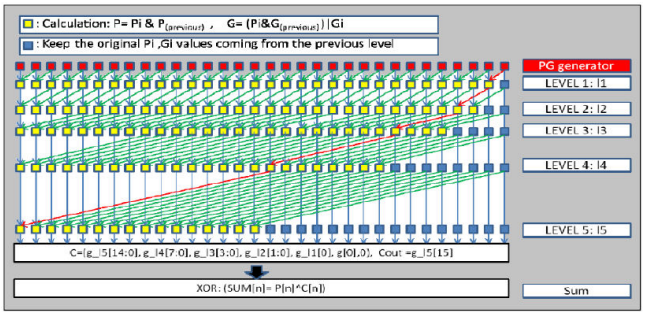

Fig 2: Kogge Stone Adder

LITERATURE SURVEY

The usage of ripple carry adders in carry select adders causes a high amount of delay during its processing. The usage of Bit Excess Converters in CSA decreases logic requirements but slightly increases the delay when compared to the regular CSA. A SQRT CSA is used here for the parallel paths for computing thus helping in reducing the overall delay. In this paper a Boolean logic based SQRT CSA is proposed [1]. A Boolean logic based CSA alone will possess a higher delay without the parallel paths provided by the square root modification. The main contribution in this is logic formulation based on data dependence and optimized carry generator (CG) and CS design. The paper puts forward a modification for carry select adder in which one of the ripple carry adder present is replaced by a bit excess converter thus highly reducing the overall area as well as the consumption of power. The square root modification is also done here to decrease the computation time and to decrease the amount of delay. Although the usage of Bit excess converter increases the delay slightly the overall performance with square root modification is better than the regular square root carry select adder. The proposed design has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay [2]. This paper involves in implementing a Brent Kung adder in a 32 bit input data with the usage of complementary pass transistor logic. Since the parallel prefix adders are much more flexible in designing, so they are primarily used in digital designing. The usage of complementary pass transistor logic, a better performance can be obtained by the usage of multiplexer in the designing of various cells. The Brent Kung adder is used here since it uses the minimum circuitry in obtaining the result. The original 16 bit design is extended to 32 bit which is implemented physically and is simulated successfully according to the paper. The area and delay results are illustrated using IRSIM and Magic tool [3]. In this paper Kogge stone and Brent Kung parallel adders are used based on degenerate pass transistor logic. The threshold problem which is faced in the pass transistor family can be minimized by the usage of complementary control signals. By using these outputs parallel prefix adders are used for a 10-transistor full adder. Parallel prefix adders are used here since there are faster than the conventional adders and are more flexible to perform the addition of higher order bits in complex circuits. They also consumes smaller area and power in comparison with the conventional RCA. The transistor level implementation of parallel prefix adders based on degenerate PTL gives better performance

compared to CPL and DPL pass transistor logic [4]. The paper proposes a carry select adder with square root modification. The modified square root carry select adder is much more efficient in terms of area, power and performance than the regular square root carry select adder. Here Binary to Excess converter is used to reduce the overall area as well as power consumption as it has a smaller number of gates when compared with the regular RCA [9]. This paper emphasizes on the modification of the carry select adder to reduce the area, power consumption and to increase its performance. The modification is done at a gate-level. This modified version of the carry select adder is designed for 8 bit, 16 bit, 32 bit and 64 bit architectures and is then compared with the conventional carry select adder with its respective architectures [10]. This paper focuses on the comparison and designs of various types of adders at the gate level. Various adders such as Ripple carry, Carry look ahead, Single stage carry skip and Carry select adders are compared with each other by both their designs and their simulations. The analysis of the adders is based on design complexity, simulation time, propagation delay and proper integration [11]. (Manikandan et.al., 2016, Sethuraman et.al., 2016, Senthil Thambi et.al., 2016, Ashok et.al., 2018, Senthilkumar et.al., 2018, Sundar and Jeganathan 2019 & 2020, Anandan et.al., 2019, Murugavel et.al., 2019, Arokiaswamy et.al., 2019 & 2020, Ganesh Babu et.al., 2020, Gomathi et.al., 2019 & 2020, Manju et.al., 2020, Leema Rose et.al., 2020).

EXISTING SYSTEM

Conventional Carry Select Adder: The Carry Select Adder is one of the fastest adders used in many data-processing processors for performing arithmetic operations. It is also used in computational systems to alleviate the problem of carry propagation delay by generating multiple carries and then selecting a carry to generate the sum.

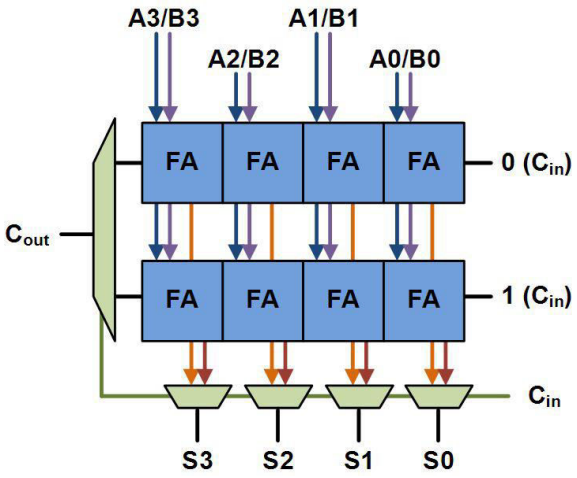

Fig 3: Conventional Carry Select Adder

Ripple Carry Adder: Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N-bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding

next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propogation delays inside the logic circuitry are the reason behind this. Propagation delay is the time elapsed between the application of an input and occurrence of the corresponding output.

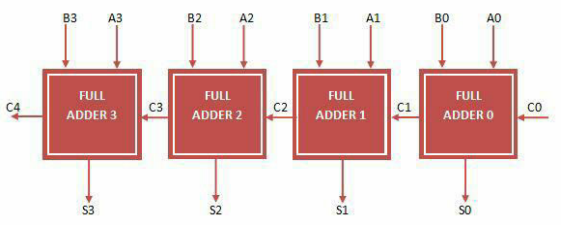

Fig 4: Ripple Carry Adder

Multiplexing is used to save I/O pins. Each display is turned ON at a rate above 100 times per second and it will appear that all the displays are turned ON at the same time due to POV(Persistence of vision).As each display is turned ON, the appropriate information must be delivered to it so that it will give the correct reading.

PROPOSED SYSTEM

Brent kung adder is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. It is a well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. The cost of development and the complexity of the wiring is lower in Brent Kung adders. The lower complexity of the gates inside the Brent Kung adder is which makes it to have lower power consumption and the reduction in the overall size of the adder.

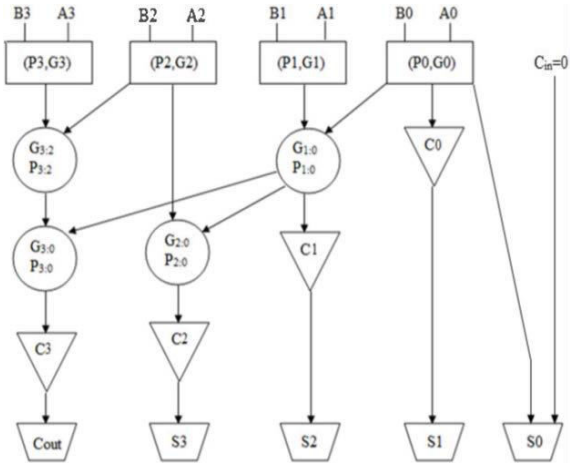

Fig 5: 4-Bit Brent Kung Adder

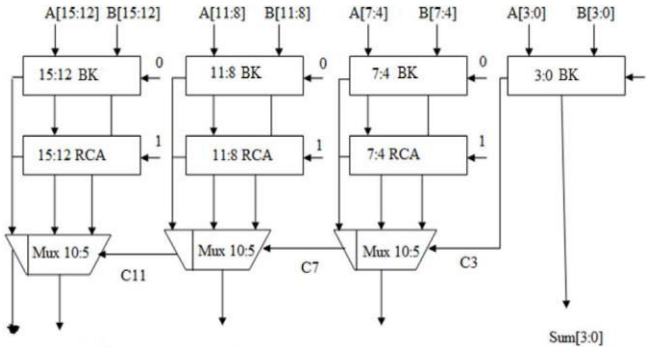

Fig 6: 16-bit Regular Linear BK Carry Select Adder

In group 2 of Regular Linear CSA, there is a single BK for C_{in}=0 and a single RCA for C_{in}=1. Now, the C3 tells whether the input carry is 0 or 1 and depending on its value, the output of particular block is selected. If C3=0, then the output of BK with C_{in}=0 is selected using 10:5 multiplexer and if C3=1 then the output of RCA with C_{in}=l is selected using the MUX. A 4-bitSum [7:4] and an output carry C7 is obtained at the output of group 2. The schematic of a 16-Bit Regular linear BK CSA is shown in the fig 6. The power and delay of this circuit is calculated.

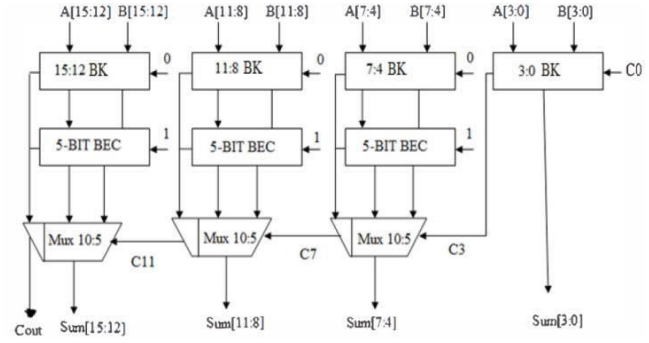

Fig 7: 16-bit Linear Modified BK Carry Select Adder

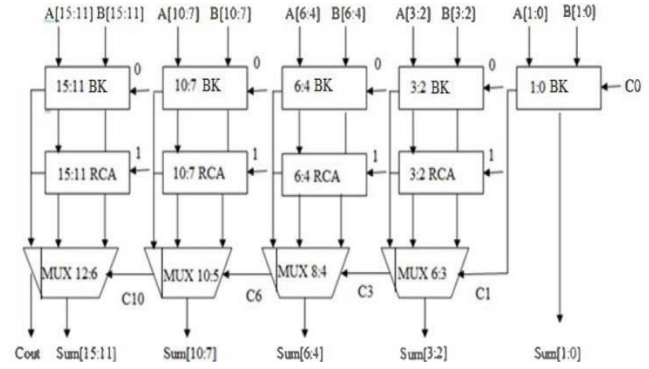

Fig 8: l6-bit Regular Square Root BK Carry Select Adder

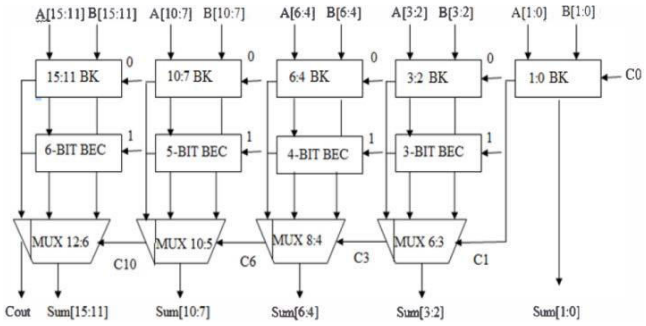

Fig 9: 16-bit Modified BK Carry Select Adder

RESULTS AND DISCUSSION

Modified Square Root Carry Select Adder with BEC reduces area and delay when compared to regular CSA. Four different architectures are designed in Tanner EDA 13.0 version tool. The simulations are performed using T-Spice with a supply voltage of 1V.The waveforms are obtained using W-Edit. The comparison for different parameters like power, delay, area and transistor count for different architectural stages for 16 bit word size is shown in table. The graphical representation for all parameters of 16 bit and 32 bit CSA word size is also shown in figure. The analysis results concluded that modified SQRT BK CSA shows better results as compared to conventional CSA and all other adder in terms of all parameters like power, delay, speed and area.

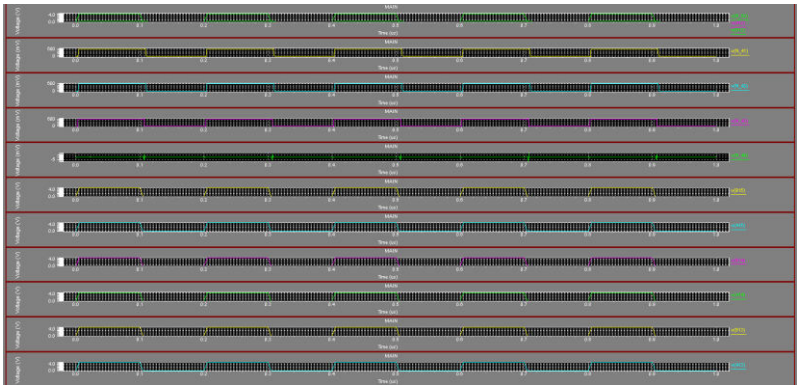

Fig 10: Fourth BK adder in the design

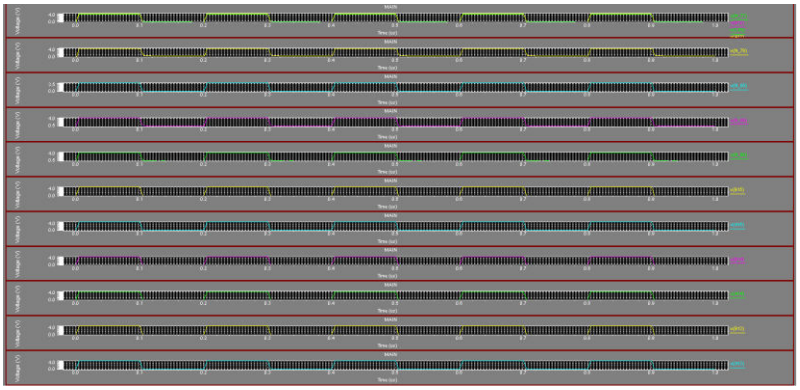

Fig 11: Third RCA in the design

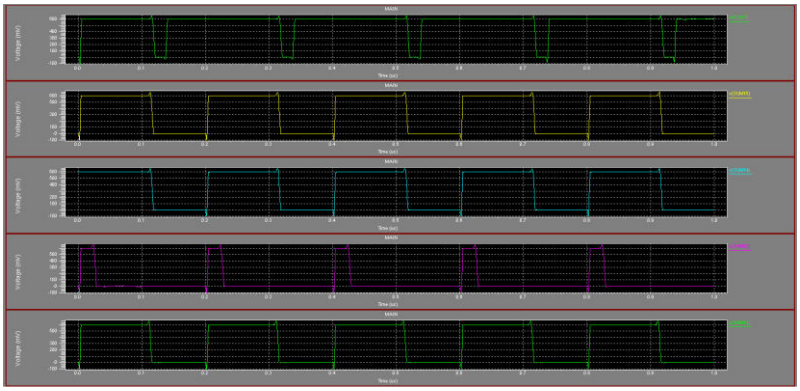

Fig 12: Third MUX in the design

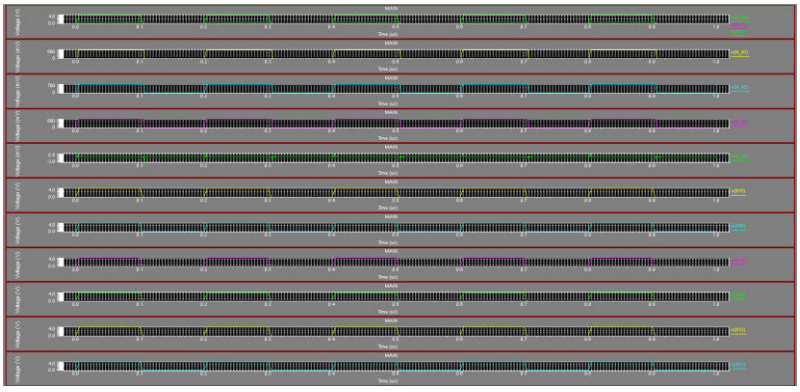

Fig 13: Fourth BK in the design

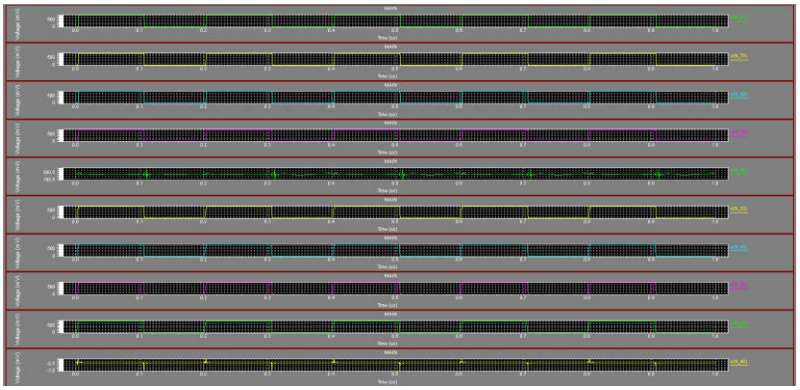

Fig 14: Third BEC in the design

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* BEGIN NON-GRAPHICAL DATA

Power Results
vdd gnd from time 0 to 1e-006
Average power consumed -> 1.000059e-005 watts
Max power 1.005297e-003 at time 5.05e-007
Min power 3.563249e-008 at time 7e-007


* END NON-GRAPHICAL DATA


* BEGIN NON-GRAPHICAL DATA

MEASUREMENT RESULTS

TRAN_Measure_Delay_1 = 2.1919e-008

* END NON-GRAPHICAL DATA
*

* Parsing                 0.01 seconds
* Setup                   0.44 seconds
* DC operating point      0.64 seconds
* Transient Analysis      7.06 seconds
* Overhead                1.19 seconds
* ----------------------------------------
* Total                   9.34 seconds

* Simulation completed  with  6 Warnings

* End of T-Spice output file
```

Fig 15: Regular Linear BK CSA Report

The analysis of the efficiency of the four architectures are done and the results are compared. Both the delays as well as the power consumption of the four architectures at different voltages are analyzed and the comparisons are as of below.

Power analysis(watts)					
VDD	0.6v	0.8v	1v	1.2v	1.4v
Regular Linear BK CSA	1.000059e-005 watts	2.870148e-005 watts	7.901268e-005 watts	2.479340e-004 watts	6.662961e-004 watts
Linear modified BK CSA	1.047172e-005 watts	1.996802e-005 watts	2.926746e-005 watts	4.540895e-005 watts	7.055567e-005 watts
Regular square root BK CSA	7.130052e-006 watts	2.845790e-005 watts	8.443072e-005 watts	2.786031e-004 watts	8.075517e-004 watts
Modified square root BK CSA	9.853889e-006 watts	2.025417e-005 watts	2.848399e-005 watts	4.319737e-005 watts	6.601233e-005 watts

Tab 1: Power analysis of the four architectures

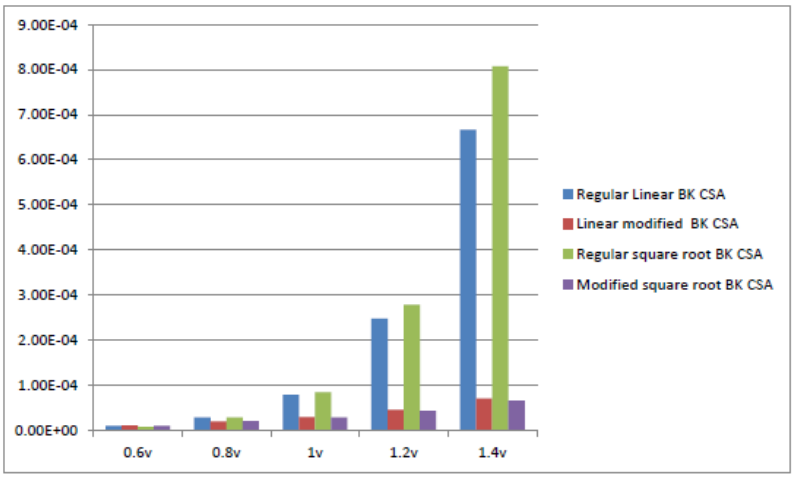

Fig 16: Power Comparison

Delay analysis(Secs)					
VDD	0.6v	0.8v	1v	1.2v	1.4v
Regular Linear BK CSA	2.2067e-008	6.8453e-009	2.4916e-009	1.4732e-009	1.1614e-009
Linear modified BK CSA	5.1343e-008	5.1057e-008	5.1592e-008	5.1739e-008	5.1124e-008
Regular square root BK CSA	4.5998e-008	4.7243e-009	5.8643e-009	8.8742e-009	4.4086e-008
Modified square root BK CSA	1.5020e-008	3.6658e-009	1.5699e-009	1.3898e-009	1.0291e-009

Tab 2: Delay analysis of the four architectures

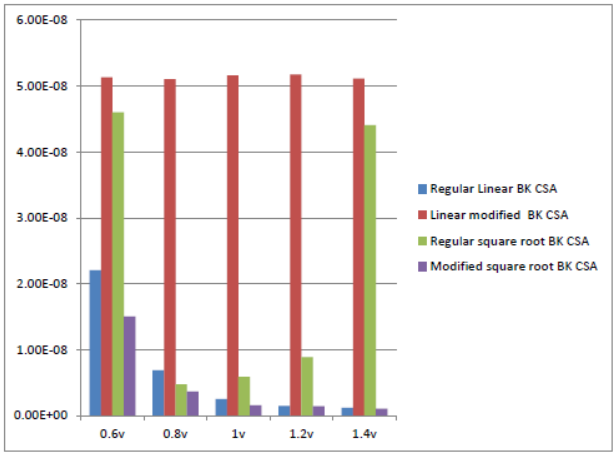

Fig 17: Delay Comparison

CONCLUSION AND FUTURE WORK

Power, delay and area are the constituent factors in VLSI design that limits the performance of any circuit. To reduce these parameters, Modified Square Root Brent Kung Carry Select Adde r(BK CSA) architecture is designed compared to other adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular Square Root BK CSA, Modified Square Root BK CSA .The circuits are designed for 16 bit word size. It can be further extended to higher order bits also. By using parallel prefix adder's area, delay and power of various structures are reduced. Results show that power consumption of Modified Square Root BK CSA is better than other structures. Transistor count is also less which indicates the design has got less area and low power. This makes it simple and efficient for VLSI network implementations.

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